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| PTO-1449 (Med. & Tech.) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. RA001C11 | SERIAL NUMBER 09/669,295 |
| | APPLICANT(S) FARMWALD ET AL. | |
| | FILING DATE September 25, 2000 | GROUP ART UNIT 2181 |

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| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
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| AA | 5,034,964 | Jul. 23, 1991 | Khan et al | | | |
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| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---------------------|--------------------|----------------|---------|-------|--------------|-----------------------|--|
| AA | SHO 58-192154 | Nov. 9, 1983 | Japan | | | NO | |
| BA | SHO 63-34795 | Feb. 15, 1988 | Japan | | | NO | |
| BA | SHO 61-107453 | May 26, 1986 | Japan | | | NO | |
| BA | SHO 63-91766 | April 22, 1988 | Japan | | | YES | |
| BA | SHO 62-16289 | Jan. 24, 1987 | Japan | | | NO | |
| AA | SHO 61-160556 | Oct. 4, 1986 | Japan | | | NO | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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| EXAMINER <i>Glen Anne</i> | DATE CONSIDERED <i>5/29/2001</i> |
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INFORMATION DISCLOSURE
STATEMENT
BY APPLICANT

ATTY. DOCKET NO.
RA001C11

SERIAL NUMBER
09/669,295

APPLICANT(S)
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U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|--------------------|----------|------------------|-------|--------------|----------------|
| BA | 4,683,735 | 05/05/87 | Novak, et. al | — | — | |
| BA | 5,684,753 | 11/04/97 | Hashimoto, et al | — | — | |
| BA | 4,322,635 | 03/30/87 | Redwine | — | — | |
| BA | 5,006,982 | 04/09/91 | Ebersole et al. | — | — | |
| BA | 4,636,986 | 01/13/87 | Pinkham | — | — | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO |
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| BA ① | Ikeda, Hiroaki et al., "100 MHz Serial Access Architecture for 4Md Field Memory," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990) |
| BA ② | Takasugi, A. et al., "A DATA TRANSFER ARCHITECTURE FOR FAST MULTI-BIT SERIAL ACCESS MODE DRAM", 11TH European Solid State Circuits Conference, Toulouse France pp. 161-165 (Sep. 1985) |
| BA ③ | Ray Pinkham et al., "A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988) |
| BA ④ | Graham, Andy et al., "Pipelined static RAM endows cache memories with 1-ns speed", Electronic Design pp. 157-170 (Dec. 1984) |
| BA ⑤ | Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," IEEE International Solid-State Circuits Conference, (Feb. 1976) |
| BA ⑥ | Pinkham, Raymond, "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984) |
| BA ⑦ | Ishimoto, S. et al., "A 256K Dual Port Memory," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985) |

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PATENT AND TRADEMARK OFFICE

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BY APPLICANT

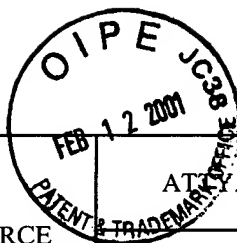
ATC DOCKET NO.
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| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
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| JA | 4,979,145 | 12/18/90 | Remington et al. | — | — | |
| JA | 5,276,846 | 01/04/94 | Aichelmann Jr., et. al | — | — | |
| JA | 4,482,999 | 11/13/84 | Janson et al. | — | — | |
| JA | 5,029,124 | 07/02/91 | Leahy et al. | — | — | |
| JA | 5,193,193 | 03/09/93 | Iyer | — | — | |
| JA | 4,926,385 | 05/15/90 | Fujishima et al. | — | — | |
| JA | 4,566,099 | 01/21/86 | Magerl | — | — | |
| JA | 4,803,621 | 02/07/89 | Kelly | — | — | |
| JA | 4,589,108 | 05/13/86 | Billy | — | — | |
| JA | 4,870,622 | 09/26/89 | Aria et al. | — | — | |
| JA | 4,878,166 | 10/31/89 | Johnson et al. | — | — | |
| JA | 4,849,965 | 07/18/89 | Chomel et al. | — | — | |
| JA | 4,851,990 | 07/25/89 | Johnson et al. | — | — | |

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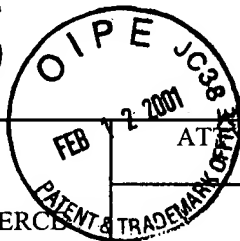
| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO |
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| JA | Sho 62-71428 | 10/05/88 | JP | — | — | YES |

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| ✓ JA ⑧ | Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989) |
| ✓ JA ⑨ | Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990) |
| ✓ JA ⑩ | Robert J. Lodi et al., "MNOS-BORAM Memory Characteristics," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976) |

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| EXAMINER <i>John Anne</i> | DATE CONSIDERED <i>5/29/2001</i> |
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U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|--------------------|----------|---------------------|-------|--------------|----------------|
| BA | 4,528,661 | 07/09/85 | Bahr et al. | — | — | |
| MA | 4,048,673 | 09/13/77 | Hendrie et al. | — | — | |
| MA | 4,519,034 | 05/21/85 | Smith et al. | — | — | |
| MA | 4,748,617 | 05/31/88 | Drewlo | — | — | |
| MA | 4,839,801 | 06/13/89 | Nicely et al. | — | — | |
| MA | 4,949,301 | 08/14/90 | Joshi et al. | — | — | |
| MA | 3,950,735 | 04/13/76 | Patel | — | — | |
| MA | 4,047,246 | 09/06/77 | Kerllenevich et al. | — | — | |
| MA | 5,029,124 | 07/02/91 | Leahy et al. | — | — | |
| MA | 4,763,249 | 08/09/88 | Bomba et al. | — | — | |
| MA | 4,625,307 | 11/25/86 | Tulpule et al. | — | — | |

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| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
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| MA | Sho 62-71428 | 10/05/88 | JP | — | — | YES | |

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| EXAMINER | Glenn Sum | DATE CONSIDERED | 5/29/2001 |
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Sheet 1 of 9

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| PTO-1449 (Modified) | APP. DOCKET NO. RA001C11 | SERIAL NUMBER 09/669,295 |
| U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | APPLICANT(S) FARMWALD ET AL. | |
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U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|--------------------|----------|-------------------|-------|--------------|----------------|
| <i>MA</i> | 4,754,433 | 06/28/88 | Chin et al. | — | — | |
| <i>MA</i> | 5,023,488 | 06/11/91 | Gunning | — | — | |
| <i>MA</i> | 4,920,486 | 04/24/90 | Nielson | — | — | |
| <i>MA</i> | 4,719,602 | 01/12/88 | Haq et al. | — | — | |
| <i>MA</i> | 4,263,650 | 04/21/81 | Bennet et al. | — | — | |
| <i>MA</i> | 3,771,145 | 11/06/73 | Wiener | — | — | |
| <i>MA</i> | 3,691,534 | 09/12/72 | Varadi et al. | — | — | |
| <i>MA</i> | 3,969,706 | 07/13/76 | Proebsting et al. | — | — | |

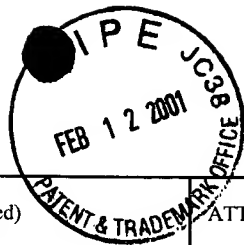
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| <i>MA</i> ① | M. Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with on-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987) |
| <i>MA</i> ② | S. Watanabe et al., "An Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982) |

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| EXAMINER <i>Glenn Anne</i> | DATE CONSIDERED <i>5/29/2001</i> |
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U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|--------------------|------------|--------------------|-------|--------------|----------------|
| RM | 4,766,536 | 8/07/23/88 | Wilson, Jr. et al. | — | — | |
| RM | 4,998,262 | 03/05/91 | Wiggers | — | — | |
| RM | 4,747,079 | 5/03/24/88 | Yamaguchi | — | — | |
| RM | 4,649,511 | 03/10/87 | Gdula | — | — | |
| RM | 4,757,473 | 07/12/88 | Kurihara et al. | — | — | |
| RM | 4,792,926 | 12/20/88 | Roberts | — | — | |
| RM | 4,811,202 | 03/07/89 | Schabowski | — | — | |
| RM | 4,860,198 | 1/07/22/89 | Takenaka | — | — | |

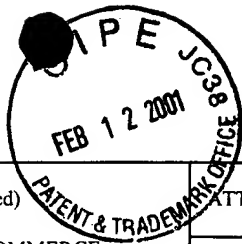
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| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. RA001C11 | SERIAL NUMBER 09/669,295 |
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U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|--------------------|----------|--------------------|-------|--------------|----------------|
| MA | 4,445,204 | 04/24/84 | Nishiguchi | — | — | |
| MA | 4,821,226 | 04/11/89 | Christopher et al. | — | — | |
| MA | 4,882,712 | 11/21/89 | Ohno et. al. | — | — | |
| MA | 4,951,251 | 08/21/90 | Yamaguchi et al. | — | — | |
| MA | 4,928,265 | 5/29/90 | Beighe et al. | — | — | |
| MA | 5,107,465 | 04/21/92 | Fung et al. | — | — | |
| MA | 4,206,833 | 04/27/93 | Lee | — | — | |
| MA | 4,953,128 | 08/28/90 | Kawai et al. | — | — | |
| MA | 5,140,688 | 08/18/92 | White et al. | — | — | |
| MA | 5,018,111 | 05/21/91 | Madland | — | — | |
| MA | 4,734,880 | 03/29/88 | Collins | — | — | |
| MA | 4,183,095 | 01/08/80 | Ward | — | — | |
| MA | 4,975,872 | 12/04/90 | Zaiki | — | — | |

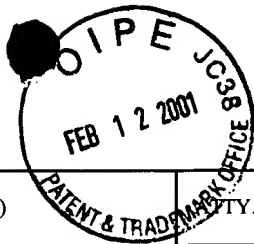
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| MA ③ | T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul., Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982) |
| MA ④ | L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983) |

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| EXAMINER Glenn Aune | DATE CONSIDERED 5/29/2001 |
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| | APPLICANT(S) FARMWALD ET AL. | |
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U.S. PATENT DOCUMENTS

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|----------------------|--------------------|----------|--------------------|-------|--------------|----------------|
| MA | 5,016,226 | 05/14/91 | Hiwada et al. | — | — | |
| MA | 5,109,498 | 04/28/92 | Kamiya et al. | — | — | |
| MA | 4,807,189 | 02/21/89 | Pinkham et al. | — | — | |
| MA | 4,092,665 | 05/30/78 | Saran | — | — | |
| MA | 4,799,199 | 01/17/89 | Scales, III et al. | — | — | |
| MA | 5,142,637 | 09/25/92 | Harlin et al. | — | — | |
| MA | 5,148,523 | 09/15/92 | Harlin et al. | — | — | |

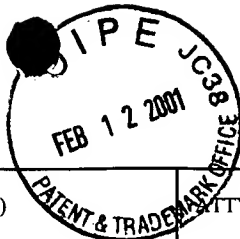
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| MA (5) | A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989) |
| MA (6) | D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5- μ m Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988) |
| MA (7) | T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988) |
| MA (8) | D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87) |
| MA (9) | F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987 |
| MA (10) | K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986) |
| MA (11) | K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990) |
| MA (12) | F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989) |

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U.S. PATENT DOCUMENTS

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|----------------------|--------------------|----------|------------------------|-------|--------------|----------------|
| DA | 5,016,226 | 05/14/91 | Hiwada et al. | — | — | |
| DA | 4,954,987 | 09/04/90 | Auvinen et al. | — | — | |
| DA | 4,675,850 | 06/23/87 | Kumanoya et al. | — | — | |
| DA | 4,788,667 | 11/29/88 | Nakano et al. | — | — | |
| DA | 4,945,516 | 07/31/90 | Kashiyama | — | — | |
| DA | 4,937,734 | 06/26/90 | Bechtolsheim | — | — | |
| DA | 4,845,664 | 07/04/89 | Aichelmann, Jr. et al. | — | — | |
| DA | 4,920,483 | 04/24/90 | Pogue et al. | — | — | |
| DA | 4,680,738 | 07/14/87 | Tam | — | — | |

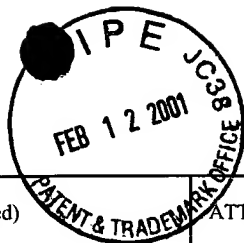
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| DA ⑬ | M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference |
| DA ⑭ | H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990) |
| DA ⑮ | D. Wendell et al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990) |
| DA ⑯ | M. Bazes et al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983) |
| DA ⑰ | R. Schmidt, "A memory Control Chip fo Formatting Data into Blocks Suitable for Video Applications", IEEE Transactions on Circuits and Systems, vol. 36, No. 10 (Oct. 1989) |
| DA ⑱ | D. K. Morgan "The CVAX CMCTL - A CMOS Memory Controller Chip", Digital Technical Journal, No. 7 (Aug. 1988) |
| DA ⑲ | T.C. Poon et al., "A CMOS DRAM-Controller Chip Implementation", IEEE Journal of Solid State Circuits, vol. 22 No. 3, pp. 491-494 (June 1987) |
| DA ⑳ | E.H. Frank "The SBUS: Sun's High Performance System Bus for RISC Workstations" Sun Microsystems Inc. 1990 |
| DA ㉑ | K. Numata et al. "New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989) |

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